Reliability and Instability of GaN MIS-HEMTs for Power Electronics

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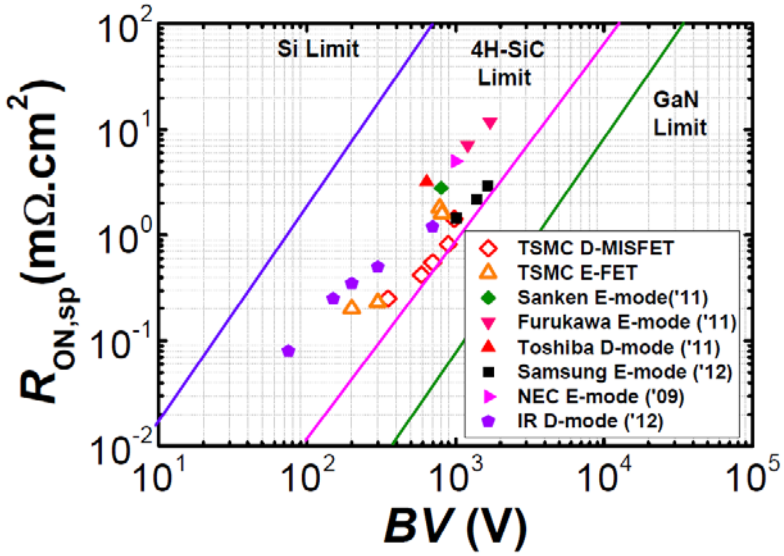
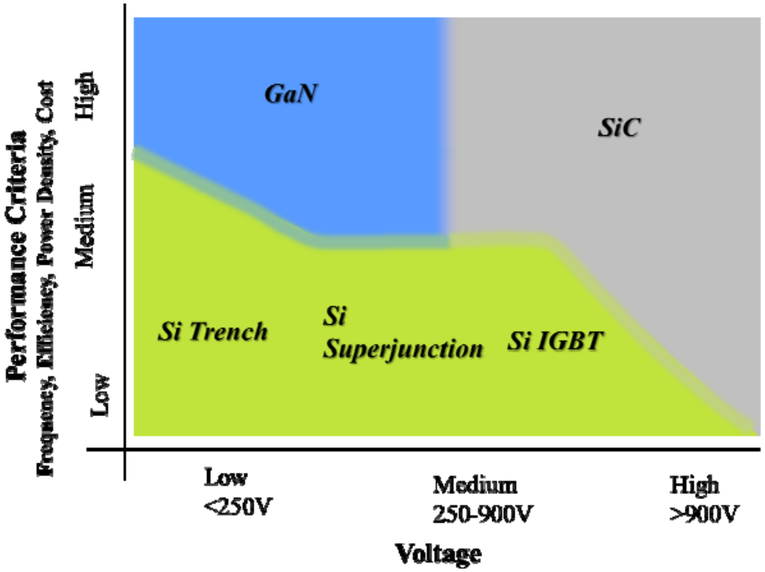
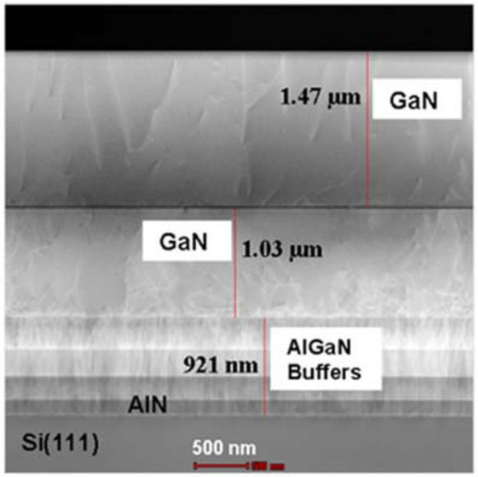
Contents

1. Introduction: GaN power electronics

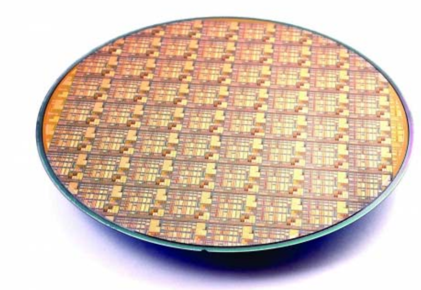




Application space for future power electronics



GaN on Si

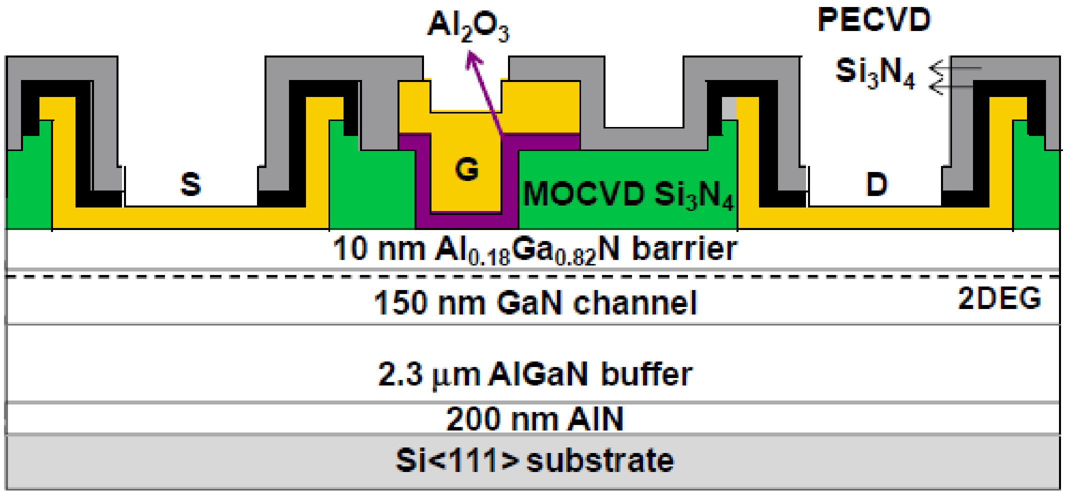


GaN MIS-HEMTs on 200 mm Si

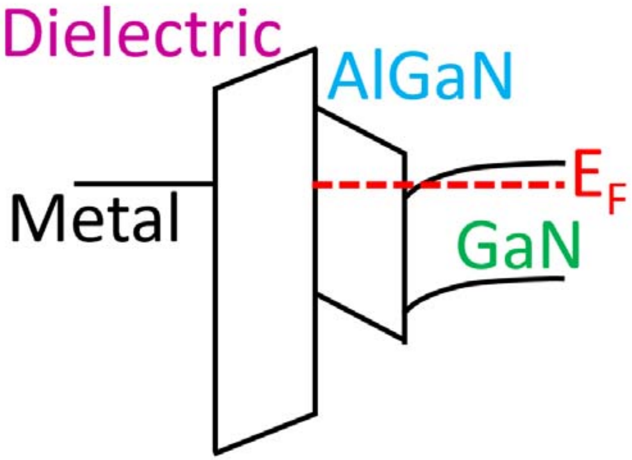
- **Opportunities**: efficiency, size, cooling
- **Challenges**: reliability, stability, ruggedness, E-mode, cost, vertical devices

Favored structure: GaN MIS-HEMT

- MIS-HEMT: Metal-Insulator-Semiconductor High Electron Mobility Transistor



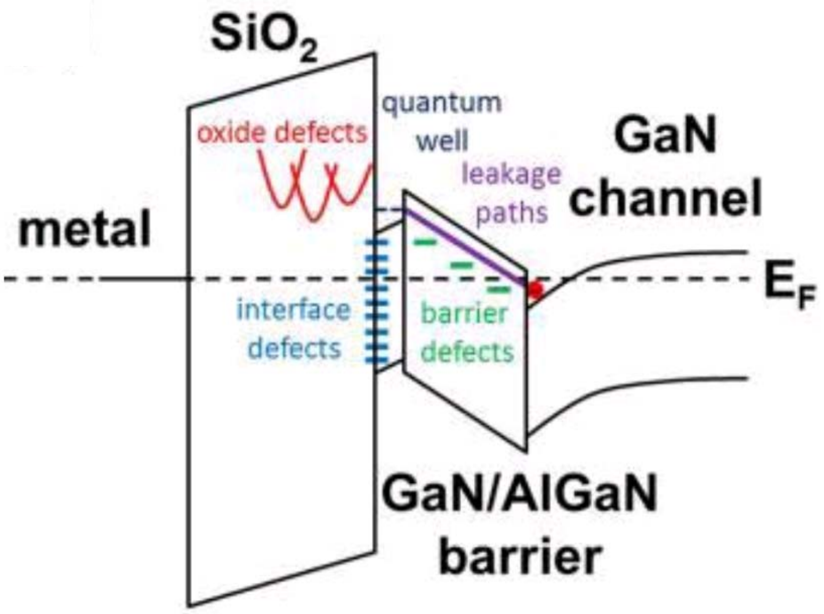
Bahl, ISPSD 2013



- High mobility 2DEG at AlGaN/GaN interface
- Dielectric to suppress gate leakage current and increase gate swing

GaN MIS-HEMT: problematic structure for reliability and stability studies

- Many interfaces, many trapping sites
- GaN cap = quantum well
- Defects in GaN substrate

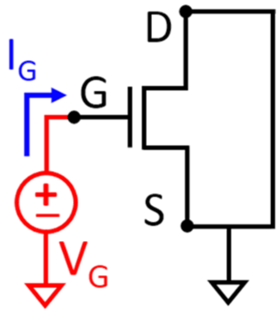


Lagger, TED 2014

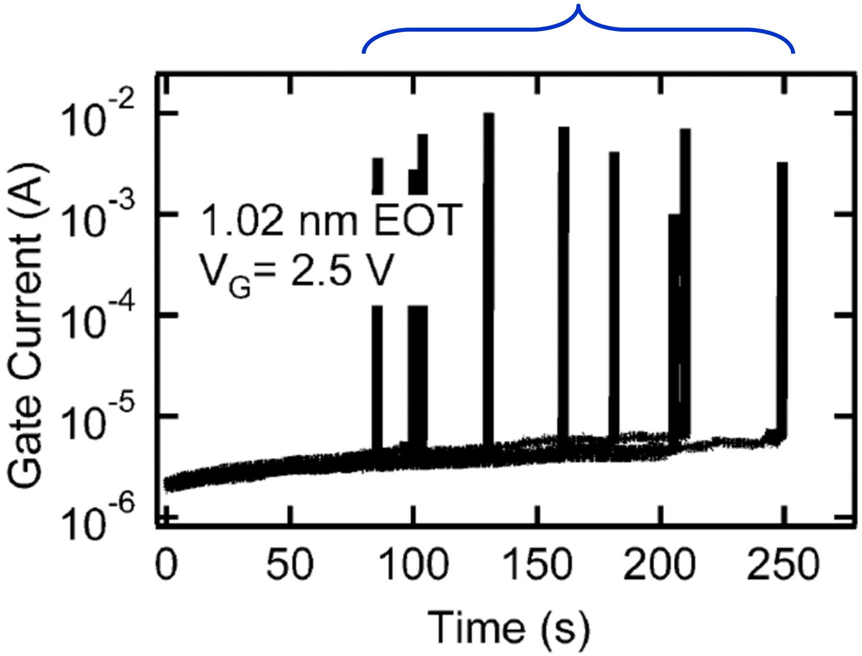
- Uncertain electric field distribution across gate stack

2. Time-Dependent Dielectric Breakdown

- High gate bias → defect generation → catastrophic oxide breakdown
- Often dictates chip lifetime

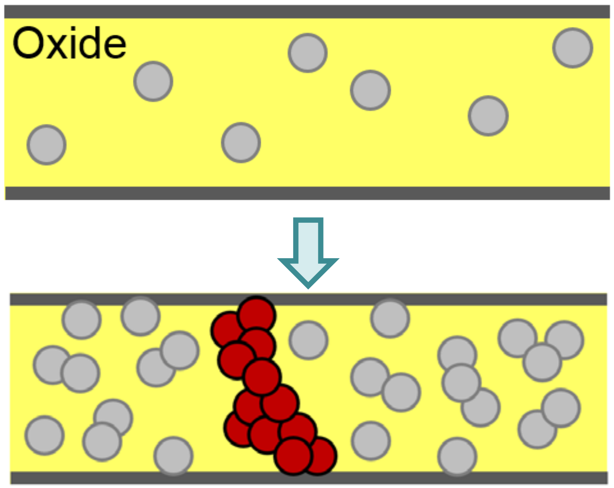


Typical TDDB experiments:
Si high-k MOSFETs



Kauerauf, EDL 2005

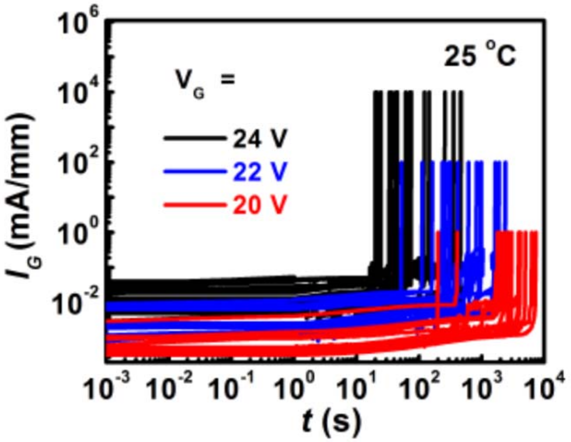
Defect formation



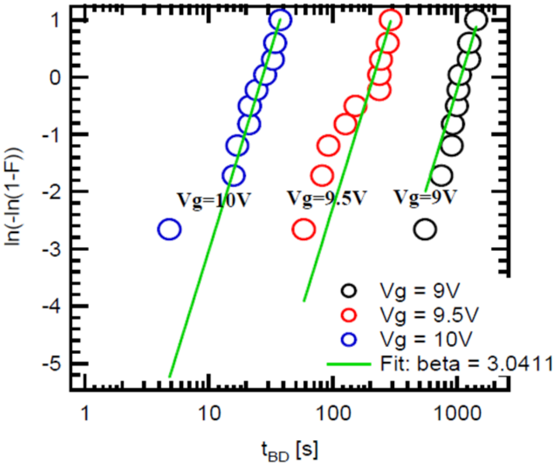
Degraeve, MR 1999

TDDB in GaN MIS-HEMTs

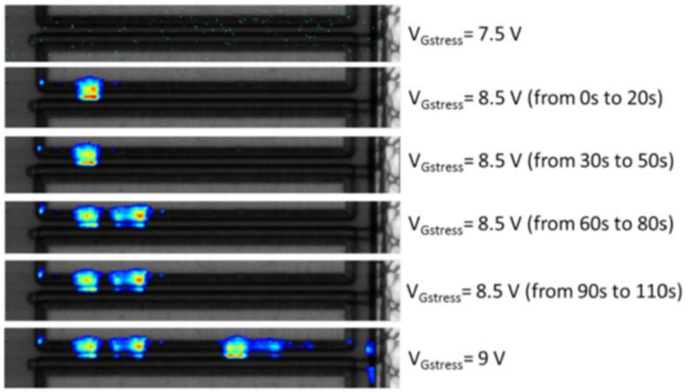
- Classic TDDB observed:



Hua, TED 2015



Wu, IRPS 2013



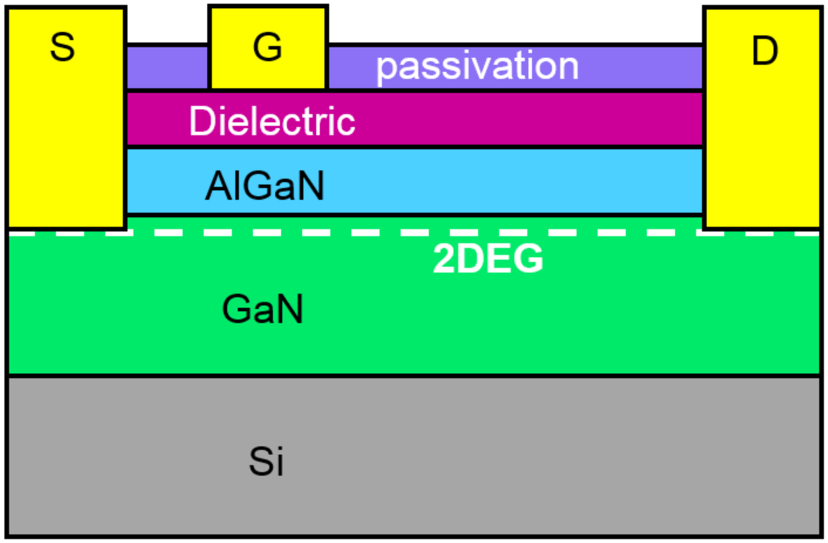
Meneghesso, SST 2016

- Studies to date focus largely on: breakdown statistics, lifetime extrapolation, evaluating different dielectrics
- **Our goal: deepening understanding of TDDB physics towards device lifetime models**

GaN MIS-HEMTs for TDDB study

GaN MIS-HEMTs from industry collaboration:

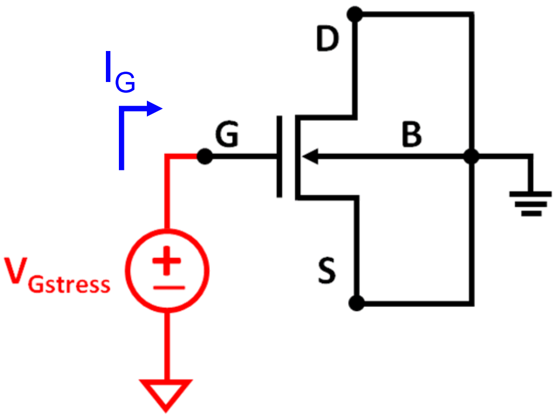
- depletion-mode
- three field-plates
- BV> 600 V
- on 6-inch Si wafers

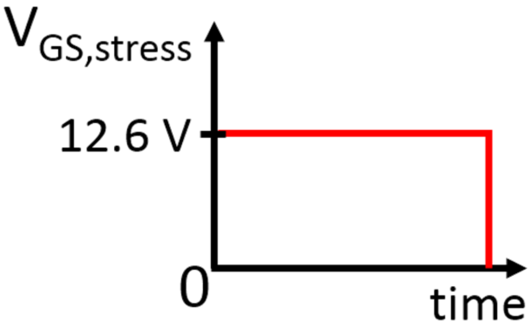


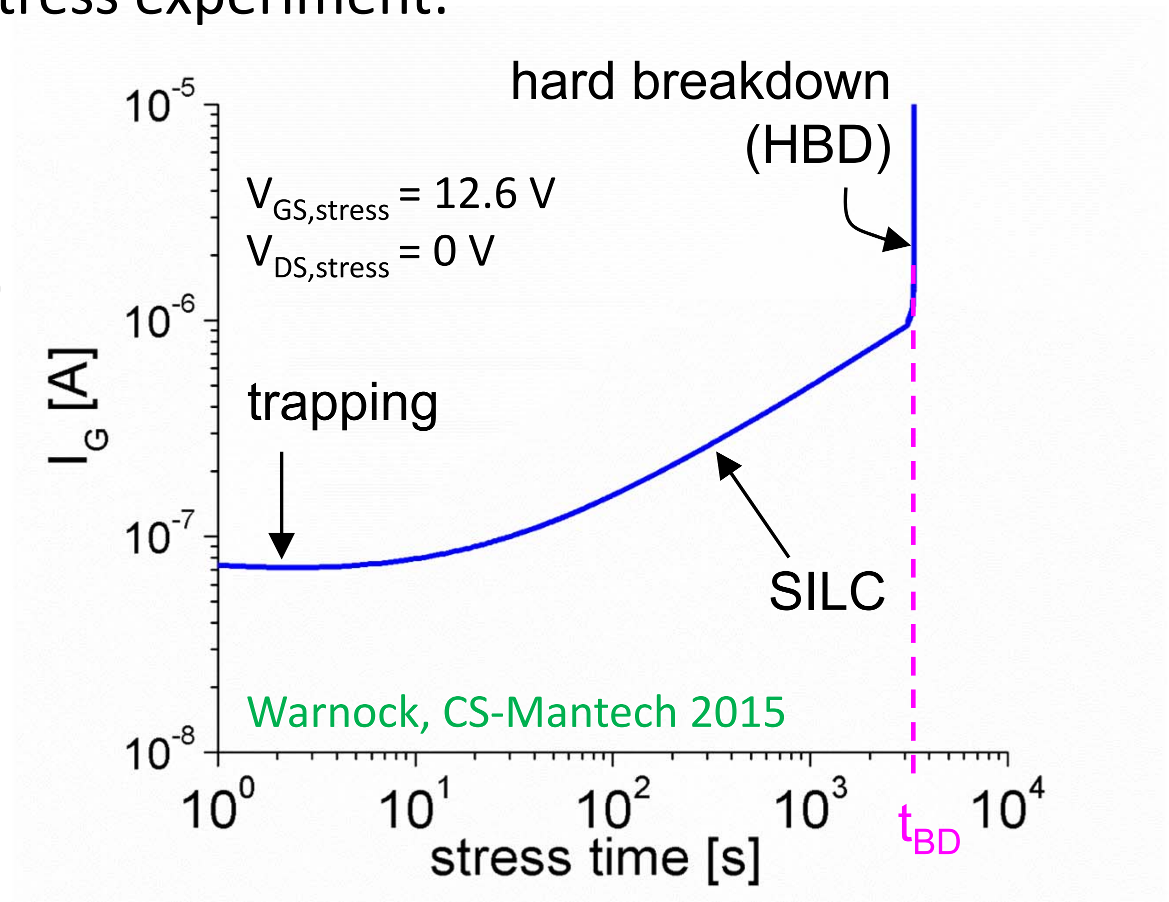
Warnock, IRPS 2016

Classic TDDB Experiment

Constant gate-voltage stress experiment:





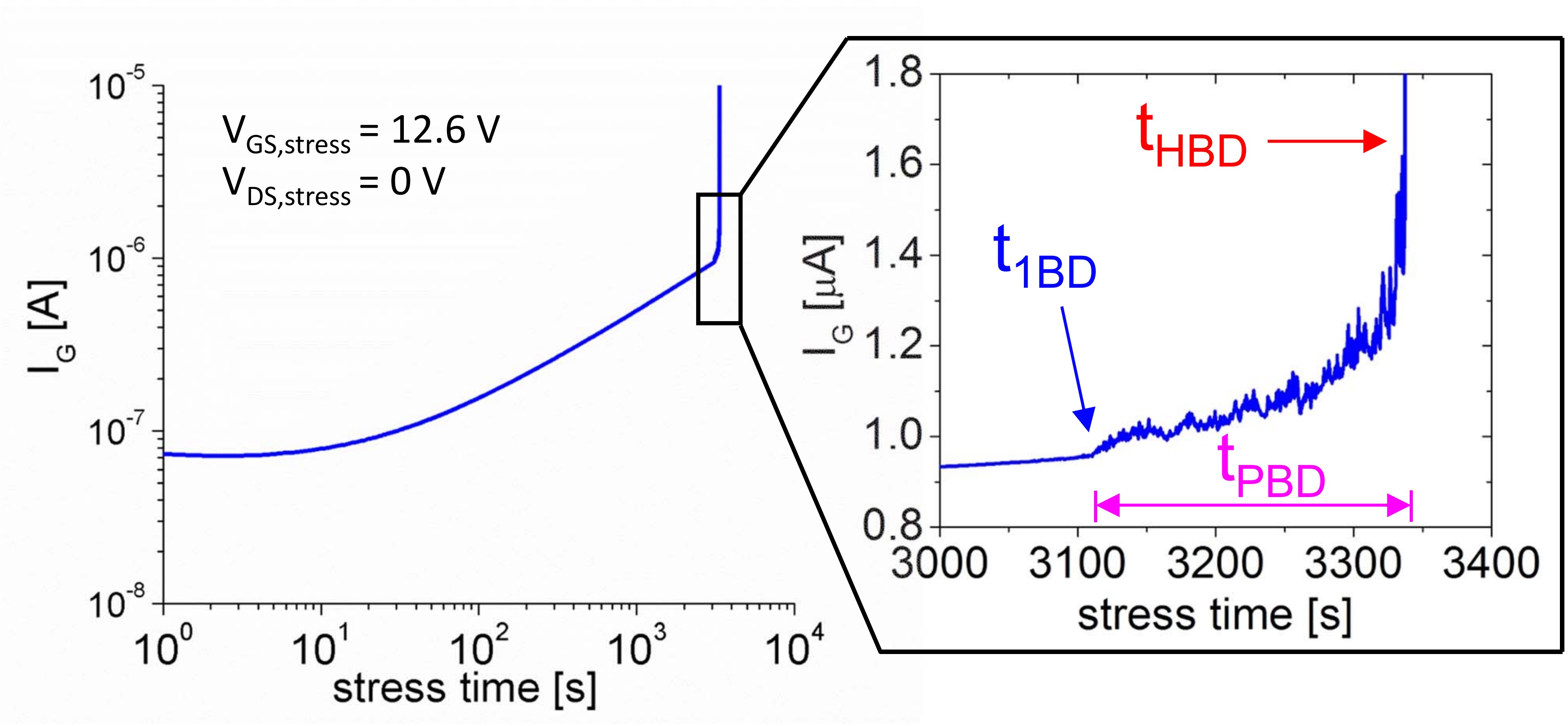


Warnock, CS-Mantech 2015

Three regimes:
- trapping
- *stress-induced leakage current* (SILC)
- dielectric breakdown

Observing Progressive Breakdown

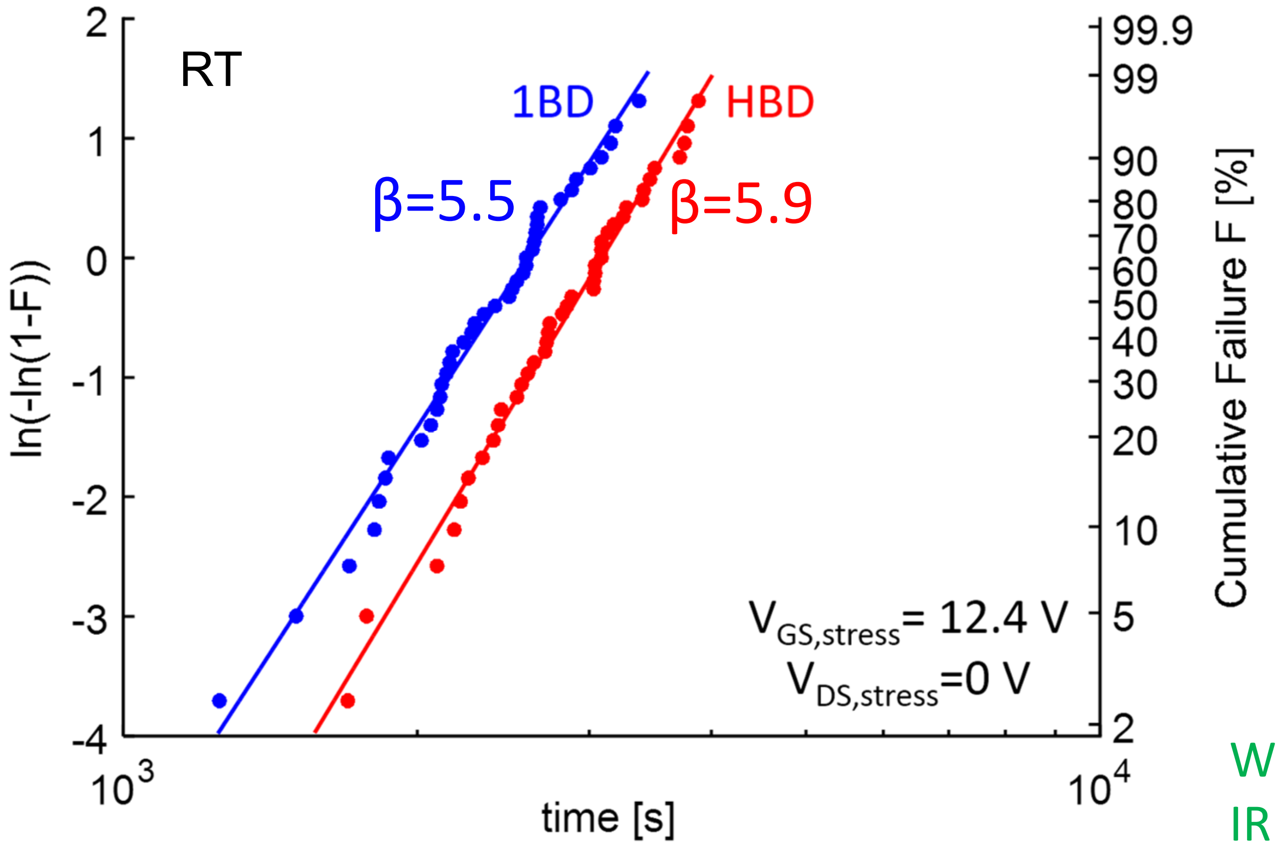
Near breakdown, I_G becomes noisy:



- Time-to-first-breakdown (1BD): I_G noise appears
- Progressive breakdown (PBD): noisy regime
- Hard breakdown (HBD): jump in I_G, device no longer operational

GaN Gate Breakdown Statistics

Statistics for time-to-first-breakdown t_{1BD} and hard breakdown t_{HBD}`

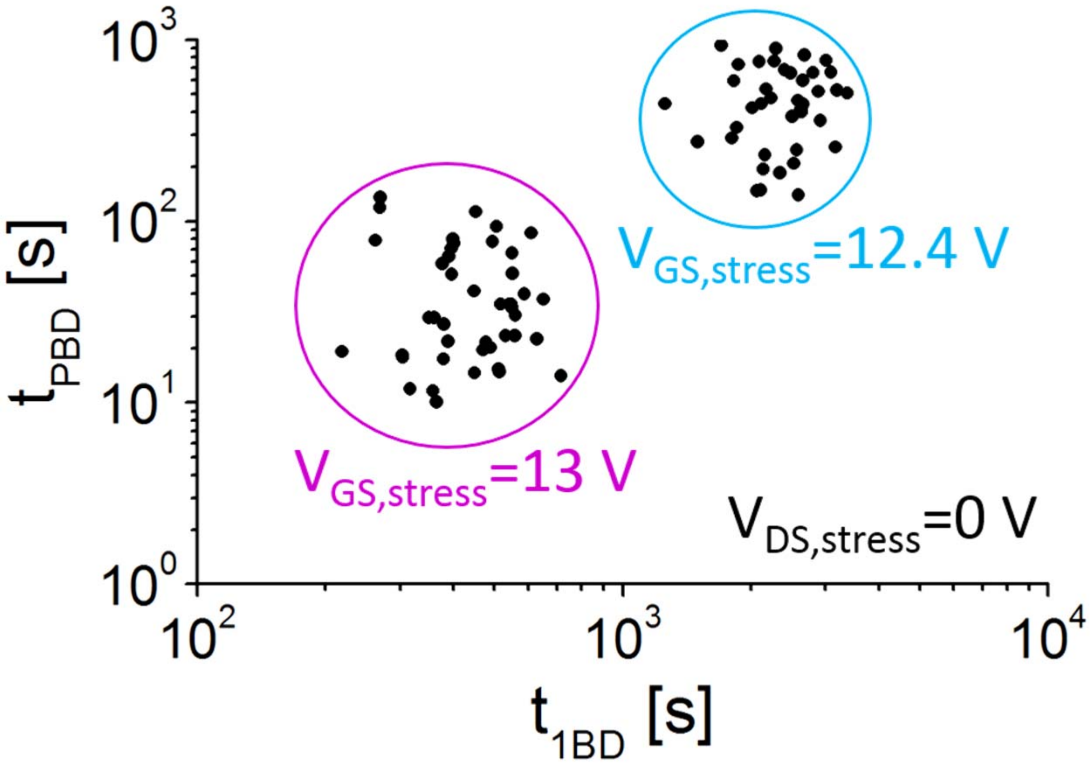


Warnock,
IRPS 2016

- *Weibull distribution*: ln[-ln(1-F)] = βln(t) - βln(η)
- Nearly parallel statistics → common origin for t_{1BD} and t_{HBD}

GaN Gate Breakdown Statistics

Time-to-first-breakdown t_{1BD} vs. PBD duration t_{PBD}



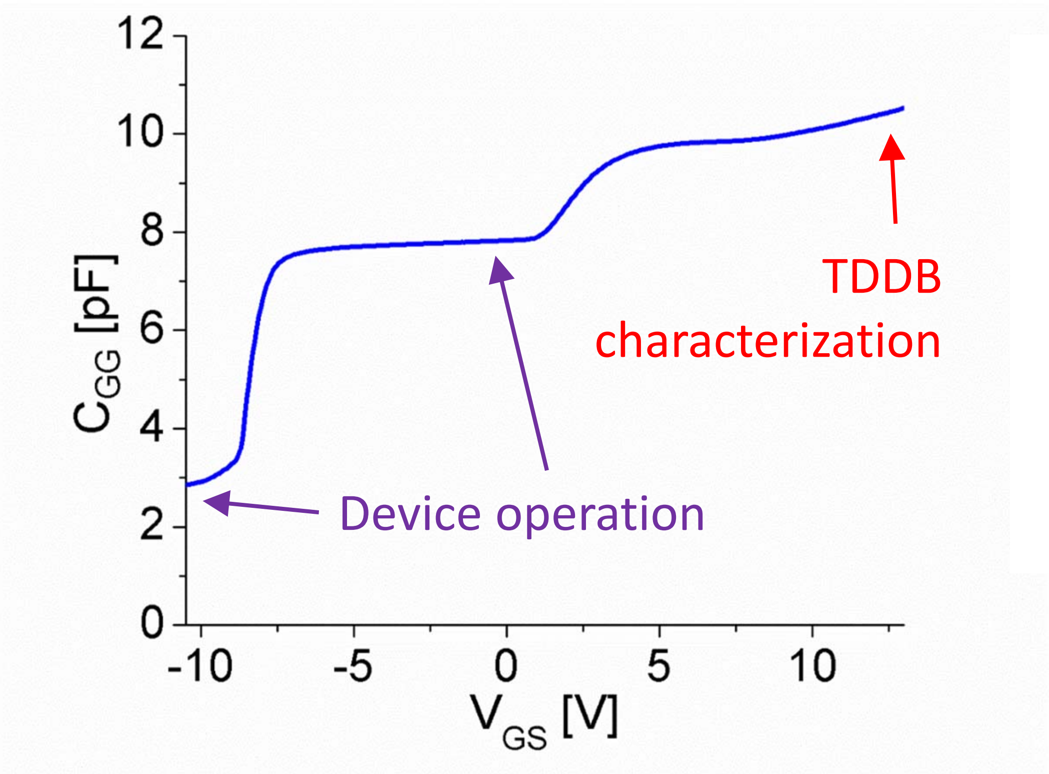
Wu, IEDM 2007

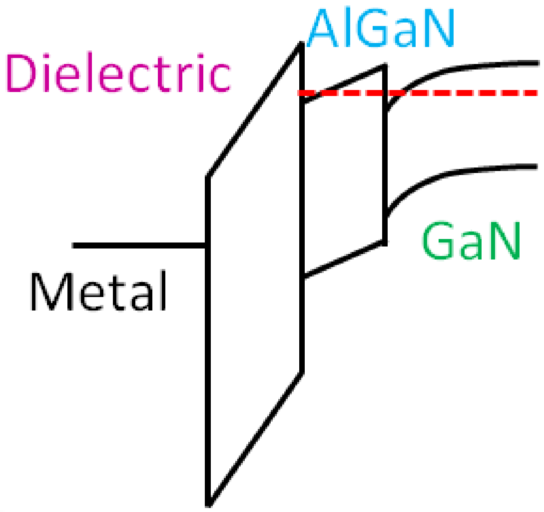
Warnock, IRPS 2016

t_{1BD} and t_{PBD} independent of one another → after first breakdown, defects generated at random until HBD occurs

Key Challenge: Lifetime Prediction

Need electric field across dielectric: gain insight through C-V characterization



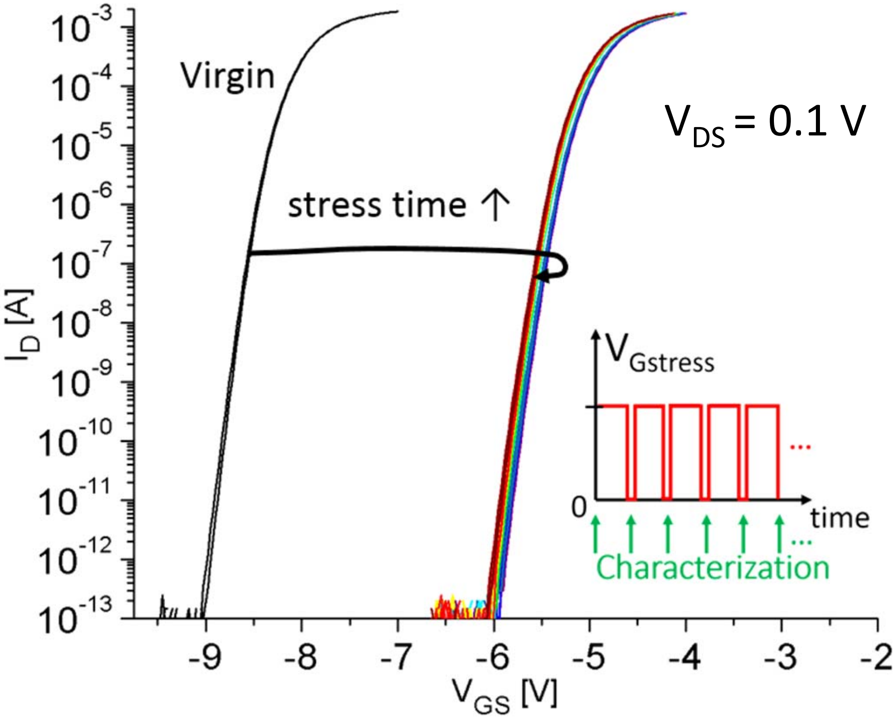


Warnock, CS-Mantech 2015

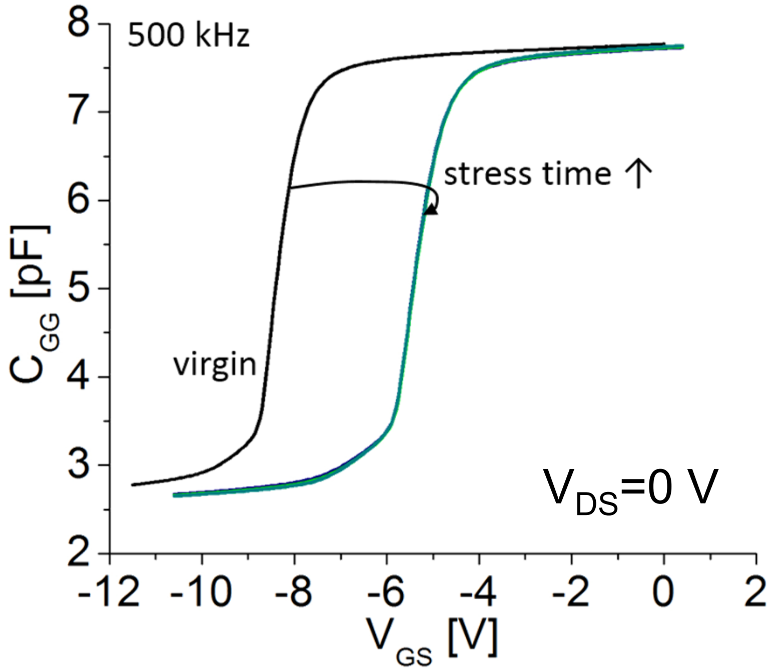
- For V_{GS}>1 V, conduction band of AlGaN barrier starts to populate
- Very different electrostatics under TDDB characterization and device operation

Key Challenge: Electric field Prediction

TDDB stress upsets electrostatics → pause stress and characterize



Warnock, CS-Mantech 2015



- Large V_T shift → trapping in dielectric or/and AlGaN
- Immediate S degradation → interface state generation early in experiment

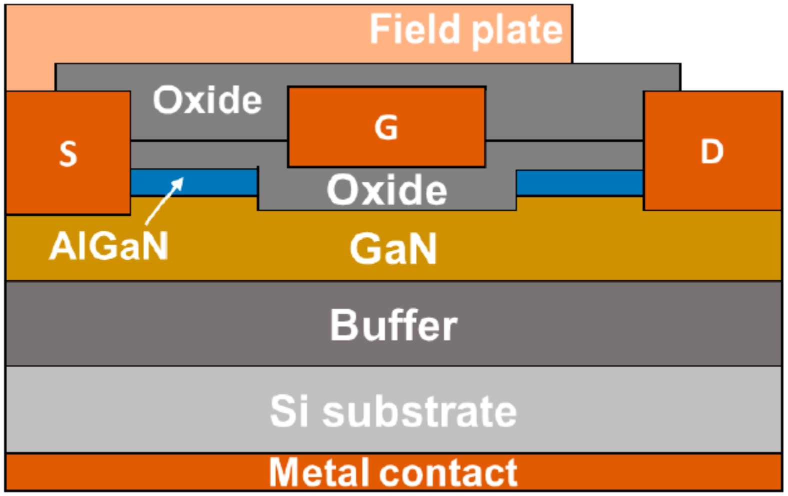
TDDB conclusions

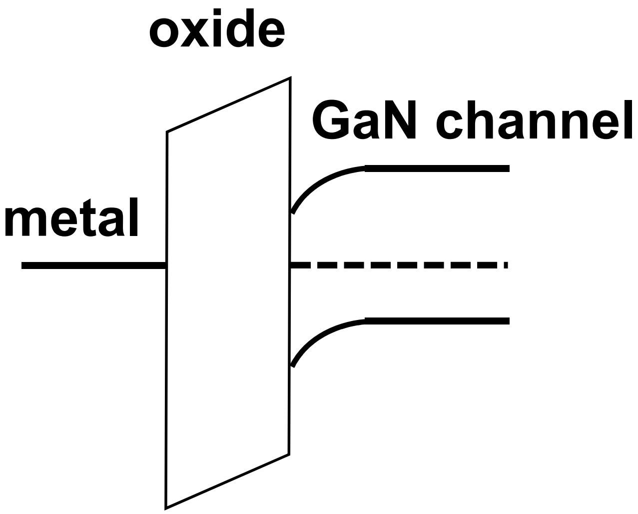
- Observed classic TDDB in GaN MIS-HEMTs:
  - Progressive breakdown followed by hard breakdown
  - Uncorrelated first breakdown and hard breakdown
  - Weibull statistics for both
- TDDB stress causes:
  - Electron pile up at dielectric/AlGaN interface
  - Prominent $\Delta V_T > 0$
  - S degradation
- Lifetime model complicated by electric field estimation

3. Bias-Temperature Instability (BTI)

- Device stability during operation: key concern, particularly V_T
- Difficult problem in GaN MIS-HEMTs

→ study simpler GaN MOSFET: single GaN/oxide interface





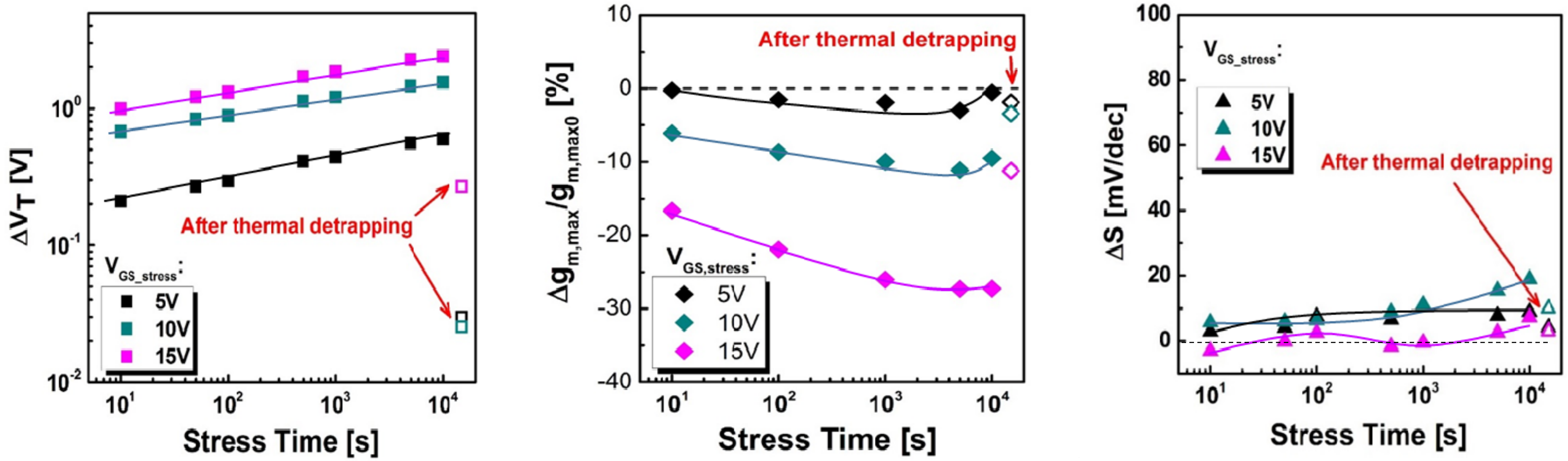
- Industrial prototype devices
- Gate dielectric: SiO_2/Al_2O_3 (EOT=40 nm)

Guo, IRPS 2015
Guo, IRPS 2016

Positive Bias Temperature Instability (PBTI)

Stress conditions: $V_{GS,stress}$ = 5, 10, 15 V; $V_{DS,stress}$=0; RT

E field ~ 1, 2, 3 MV/cm



- t_{stress} ↑ or V_{GS_stress} ↑ → ΔV_T ↑, $g_{m,max}$ ↓
- Minimal ΔS
- Near full recovery after final thermal detrapping (except for 15 V)

Guo, IRPS 2015

PBTI: Mechanisms

Study separately recoverable and non-recoverable components of ΔV_T and Δg_m:

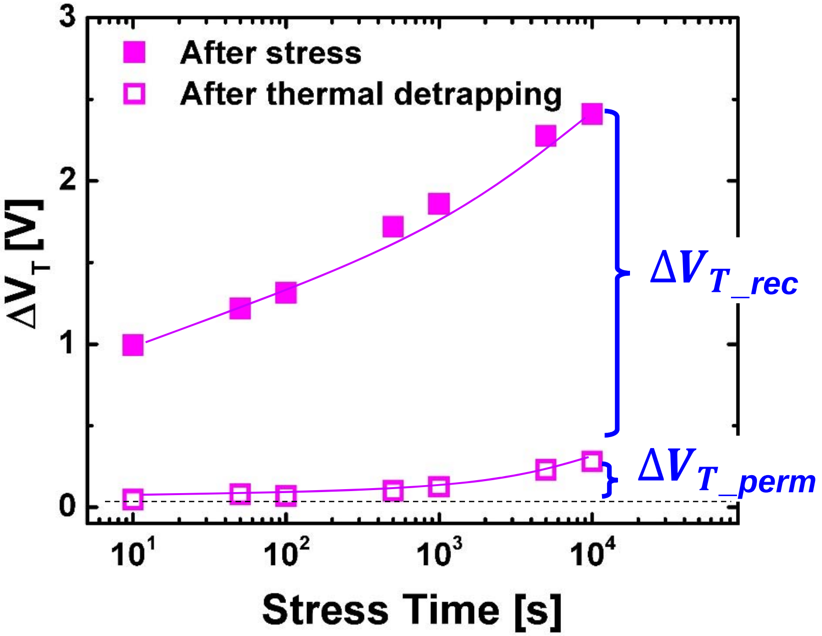
$$\Delta V_T = \Delta V_{T\_rec} + \Delta V_{T\_perm}$$

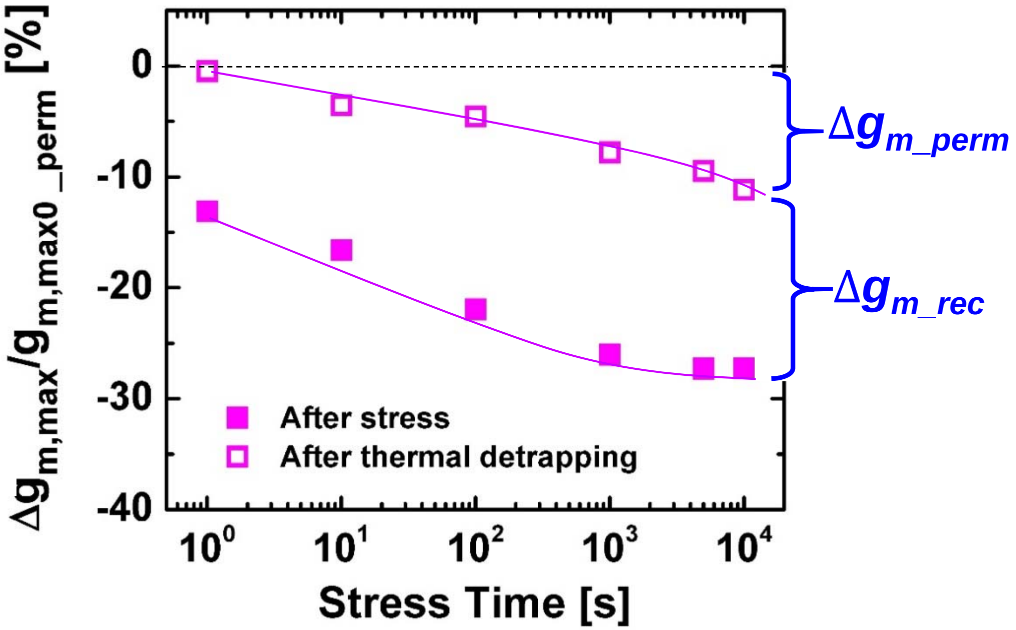
$$\Delta g_m = \Delta g_{m\_rec} + \Delta g_{m\_perm}$$

recoverable

non-recoverable = permanent

V_{GS_stress} = 15 V at RT



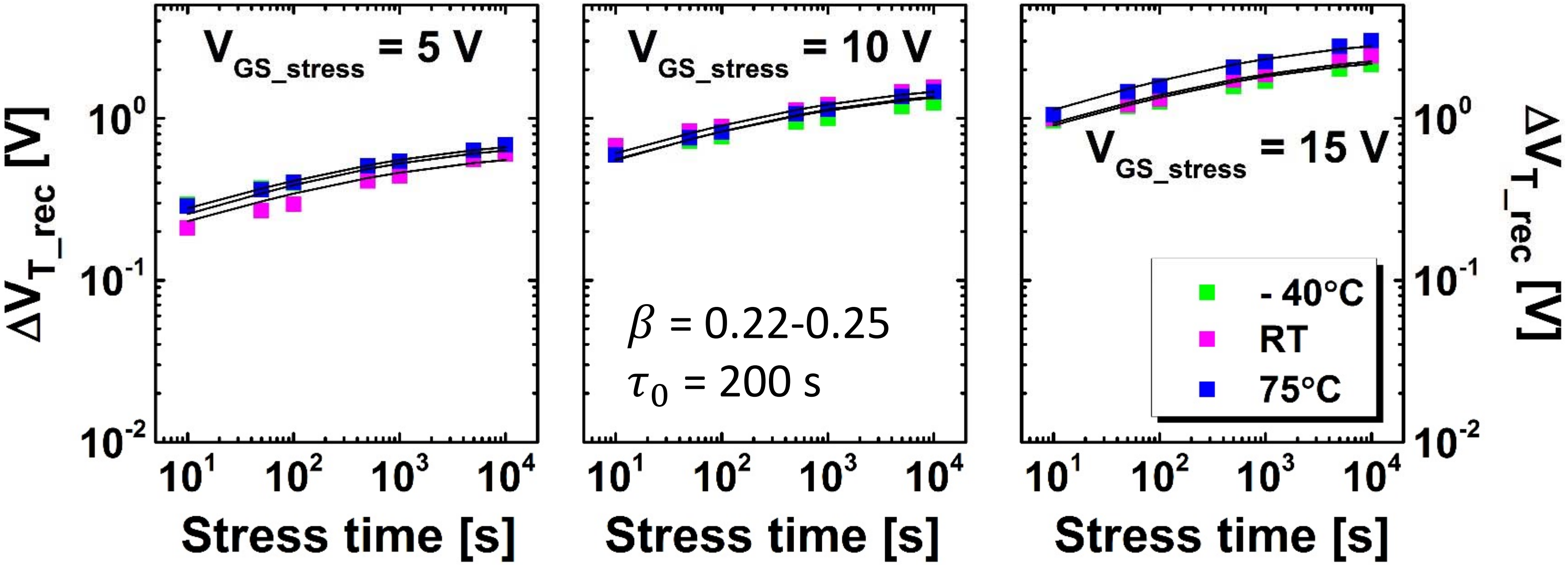


PBTI: Recoverable degradation

V_{T_rec} well described by *saturating power-law function*:

$$\Delta V_{T\_rec} = \Delta V_{max} \cdot \left\{1 - \exp\left(-\left(\frac{t}{\tau_0}\right)^{\beta}\right)\right\}$$

Zafar, TDMR 2005



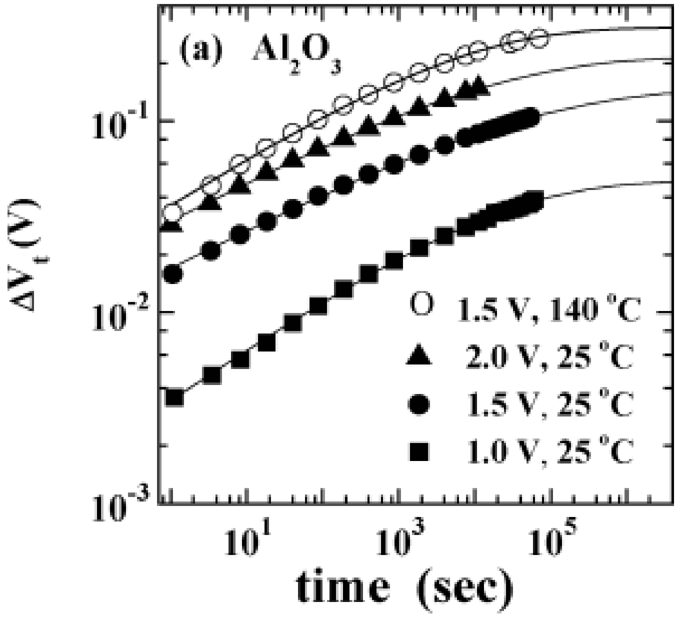
β = 0.22-0.25
τ_0 = 200 s

- Consistent with electron trapping in oxide
- Trapping takes place by tunneling

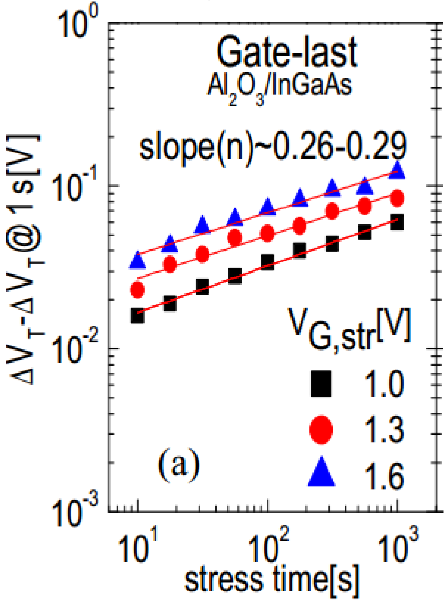
PBTI: Recoverable degradation

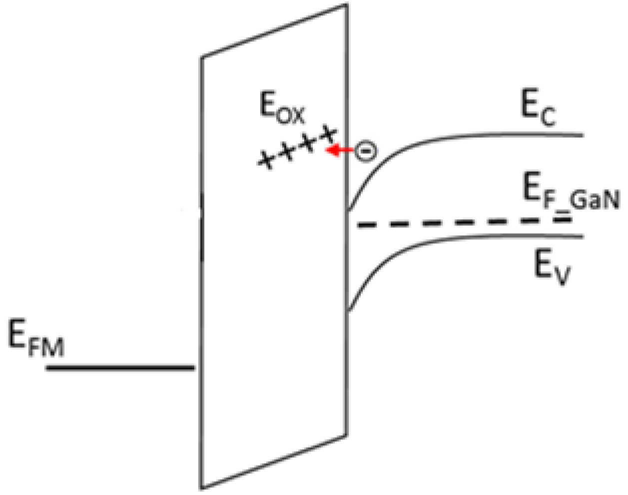
Similar to other MOS systems

Al_2O_3/Si



Al_2O_3/InGaAs





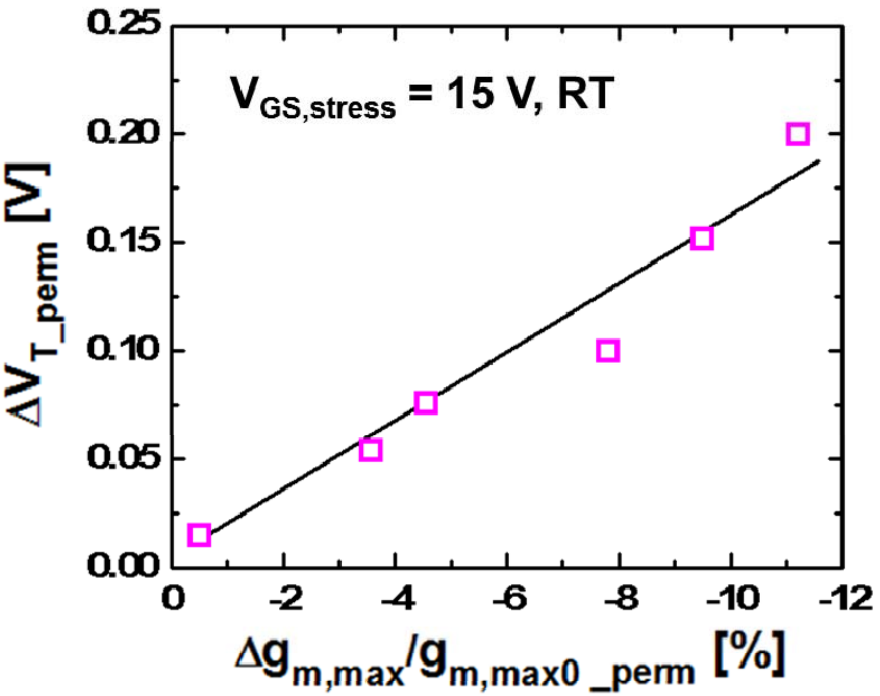
Zafar, TDMR 2005

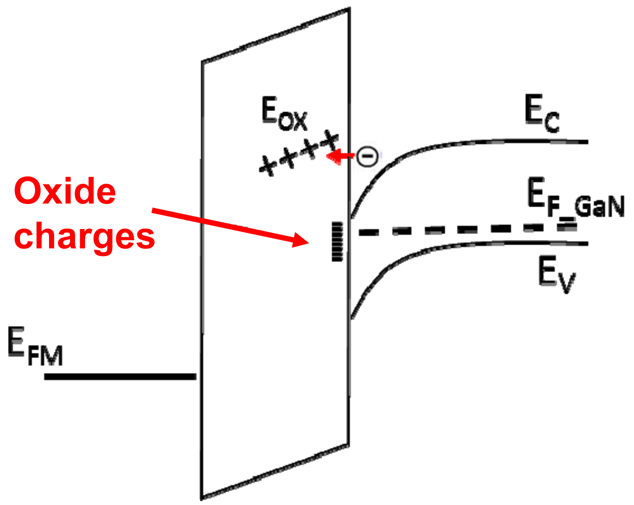
Deora, IPRS 2014

Channel	Oxide	*β*
Si	**Al_2O_3**	**0.32**
InGaAs	**Al_2O_3, ZrO_2/Al_2O_3**	**0.26-0.29**
GaN (this work)	**SiO_2/Al_2O_3**	**0.22-0.25**

PBTI: Permanent degradation

Permanent ΔV_T and Δg_m correlated:

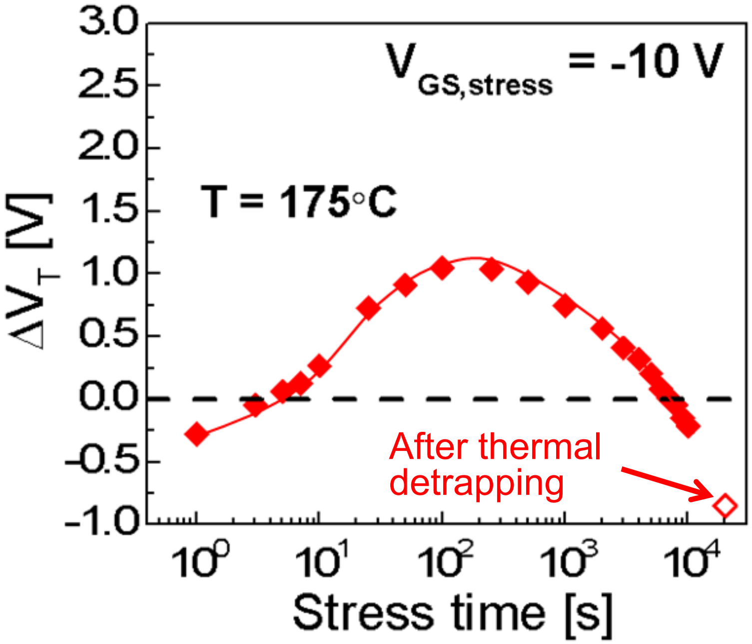




- Generation of oxide traps near Al_2O_3/GaN interface
- But… could thermal detrapping not be completely effective?

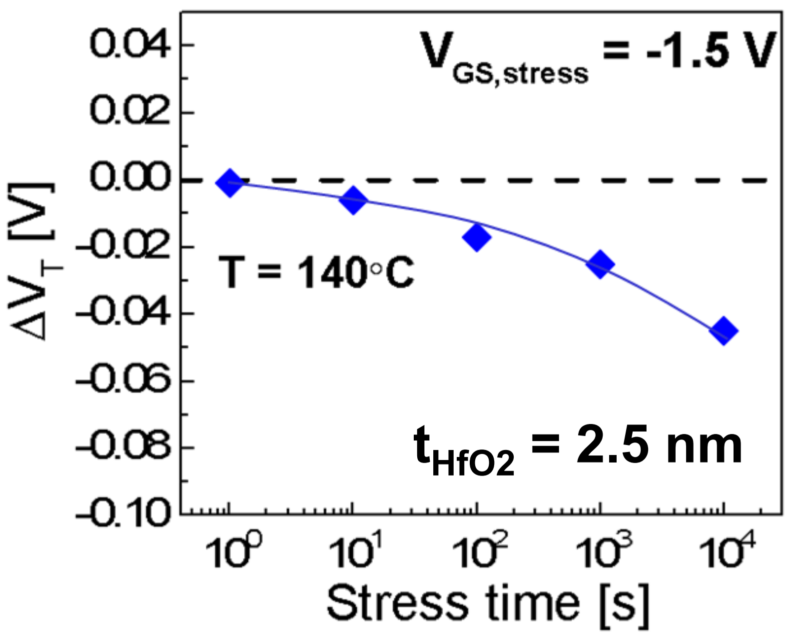
Negative Bias Stress Instability (NBTI)

This work: GaN MOSFET



Guo, IRPS 2016

Si HKMG p-MOSFET

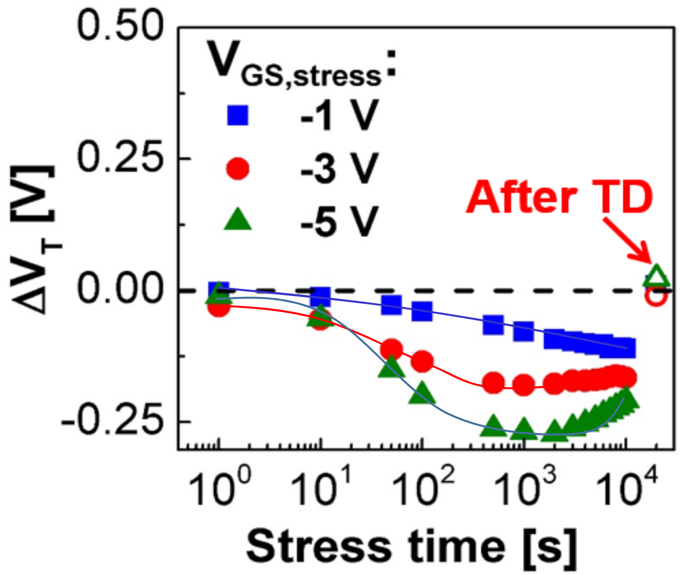


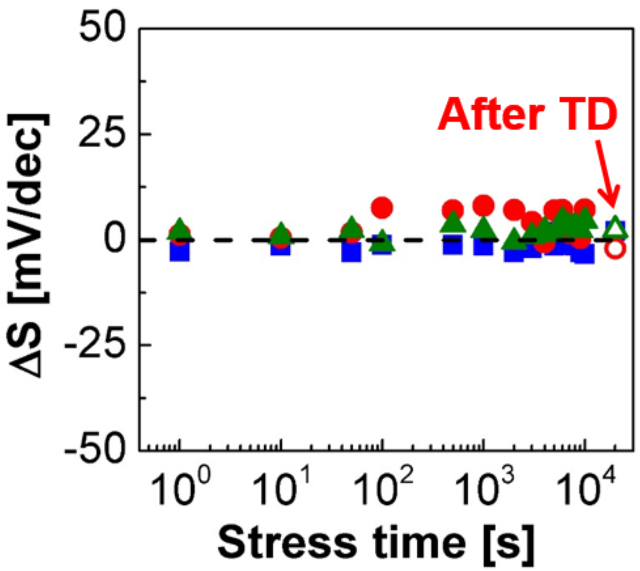
Zafar, TDMR 2005

- Three regimes: Negative ΔV_T → positive ΔV_T → negative ΔV_T
- Permanent negative ΔV_T after final thermal detrapping

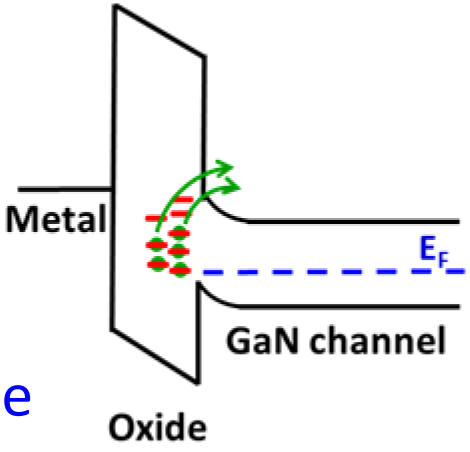
NBTI: Regime 1 (low stress)

Stress conditions: $V_{GS,Stress}$ = -1, -3, -5 V; $V_{DS,stress}$=0; RT





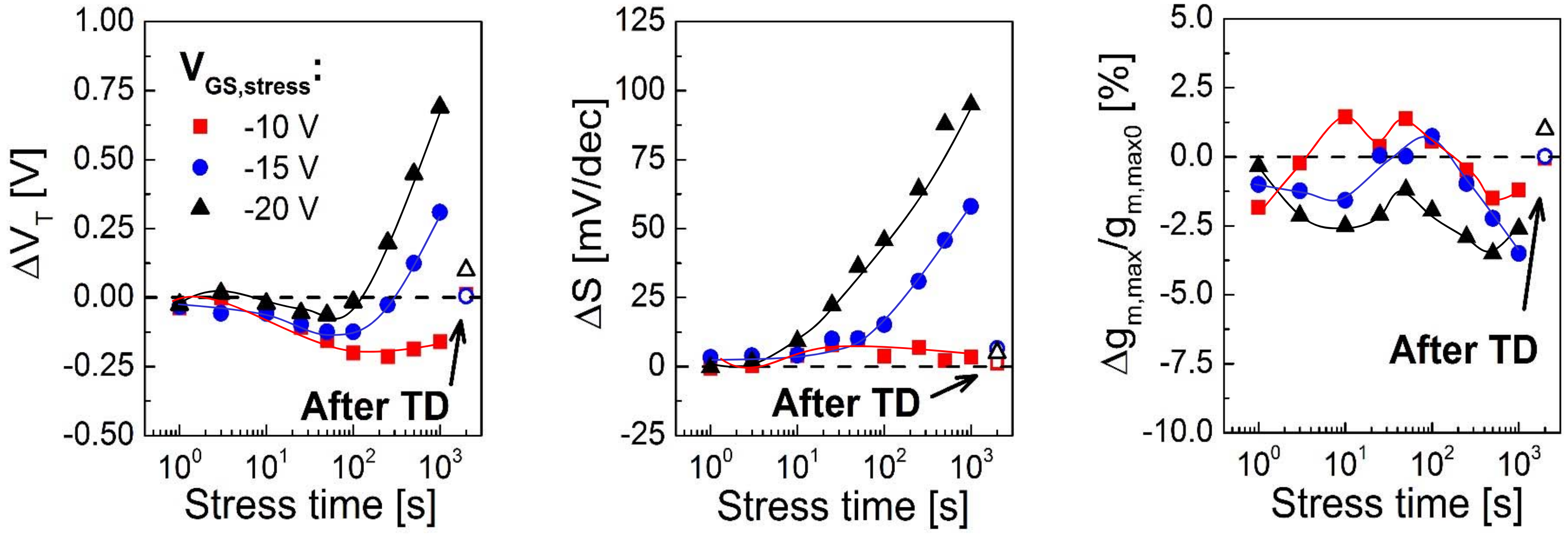
- $\Delta V_T < 0$
- $|\Delta V_T|$ increases with t_{stress} and $|V_{GS,stress}|$
- Minimal ΔS
- Complete recovery
- Consistent with electron detrapping from oxide



Meneghini, EDL 2016

NBTI: Regime 2 (mid stress)

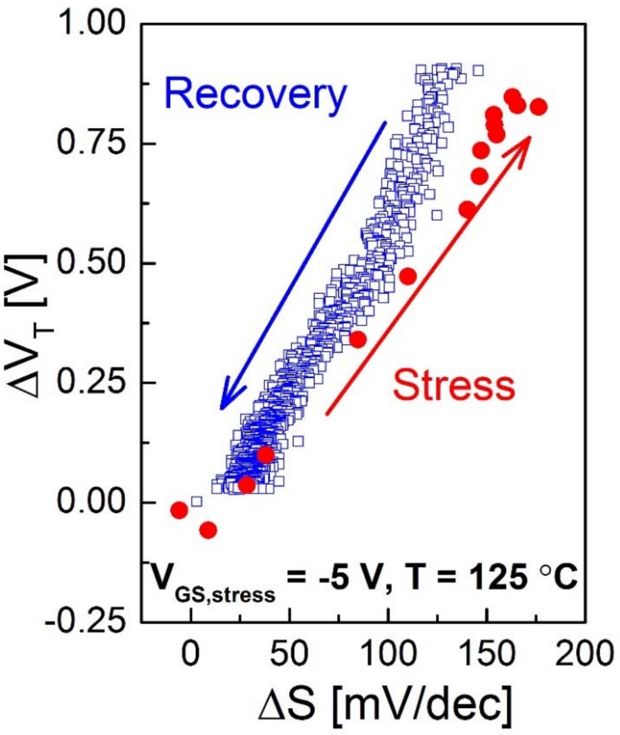
Stress conditions: $V_{GS,stress}$ = -10, -15, -20 V; $V_{DS,stress}$=0; RT

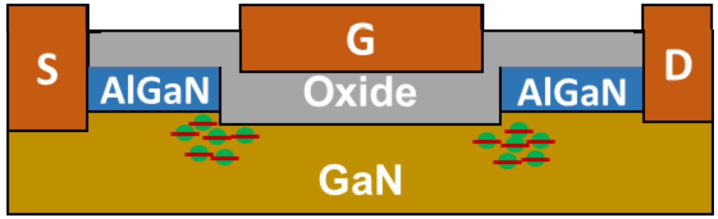


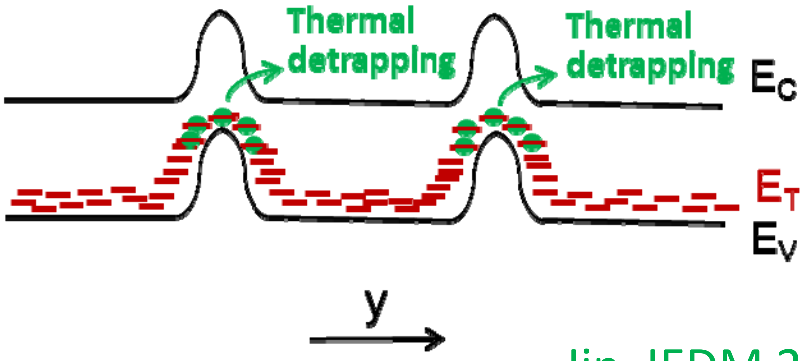
- $\Delta V_T > 0$
- $|V_{GS,stress}| \uparrow$, $t_{stress} \uparrow \rightarrow \Delta V_T \uparrow$, $\Delta S \uparrow$, $|\Delta g_{m,max}| \uparrow$
- ΔV_T , ΔS and $|\Delta g_{m,max}|$ mostly recoverable

NBTI: Regime 2 (mid stress)

ΔV_T and ΔS correlated throughout entire experiment:





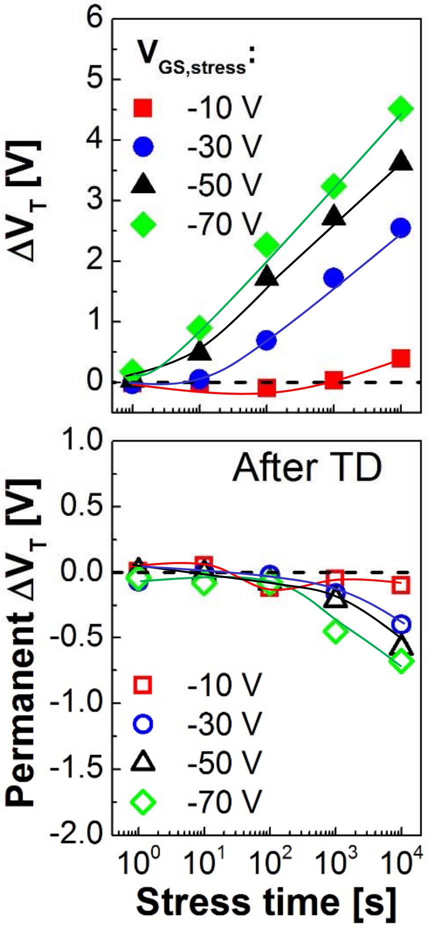


Jin, IEDM 2013

- High field at edges of gate → electron trapping in GaN substrate
- Energy bands at surface of GaN channel ↑ → positive ΔV_T, ΔS
- Thermal process effective in electron detrapping

NBTI: Regime 3 (harsh stress)

Stress conditions: $V_{GS,stress}$ = -10, -30, -50, -70 V; $V_{DS,stress}$=0; RT

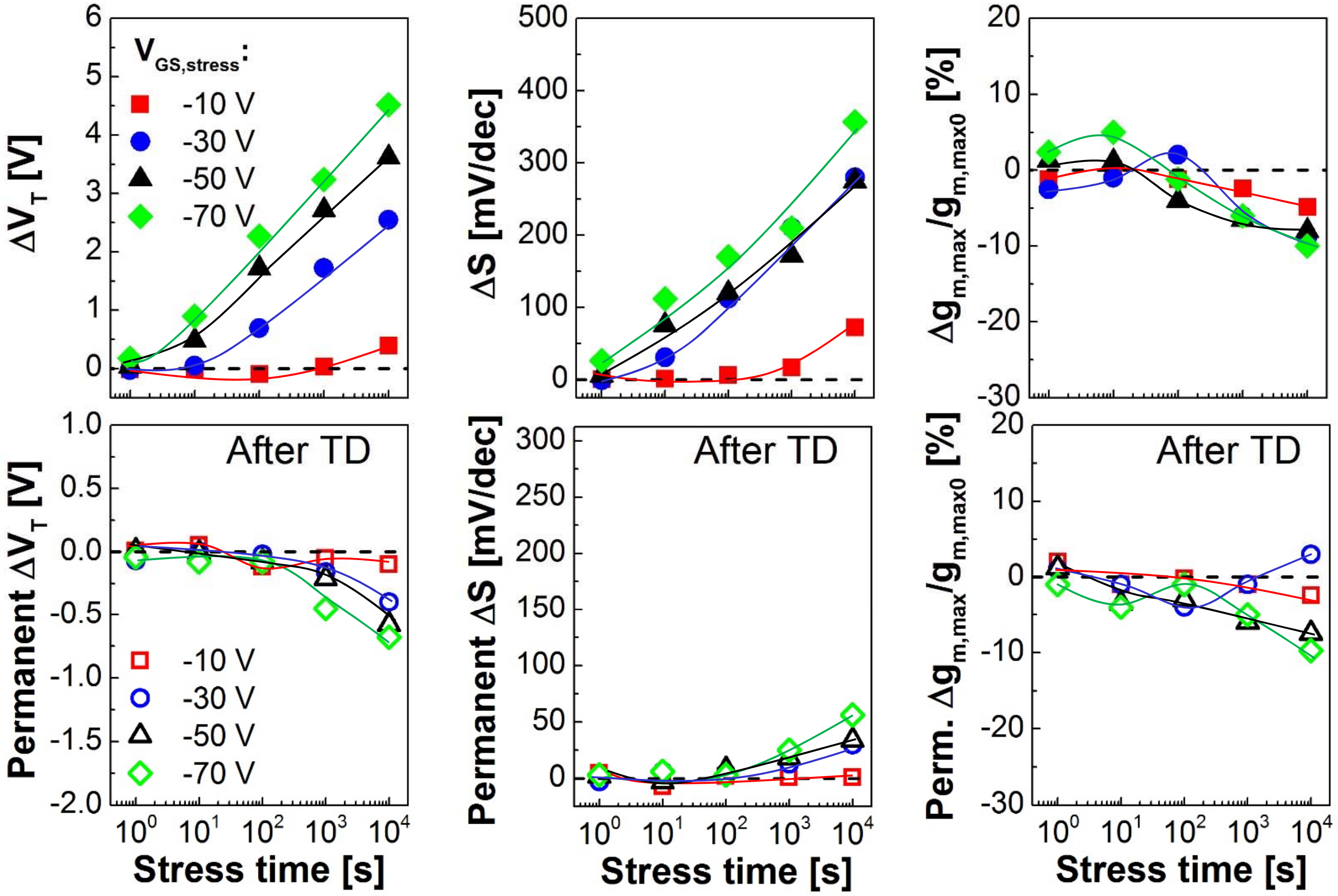


→ Similar to regime 2

→ Additional permanent negative ΔV_T

NBTI: Regime 3 (harsh stress)

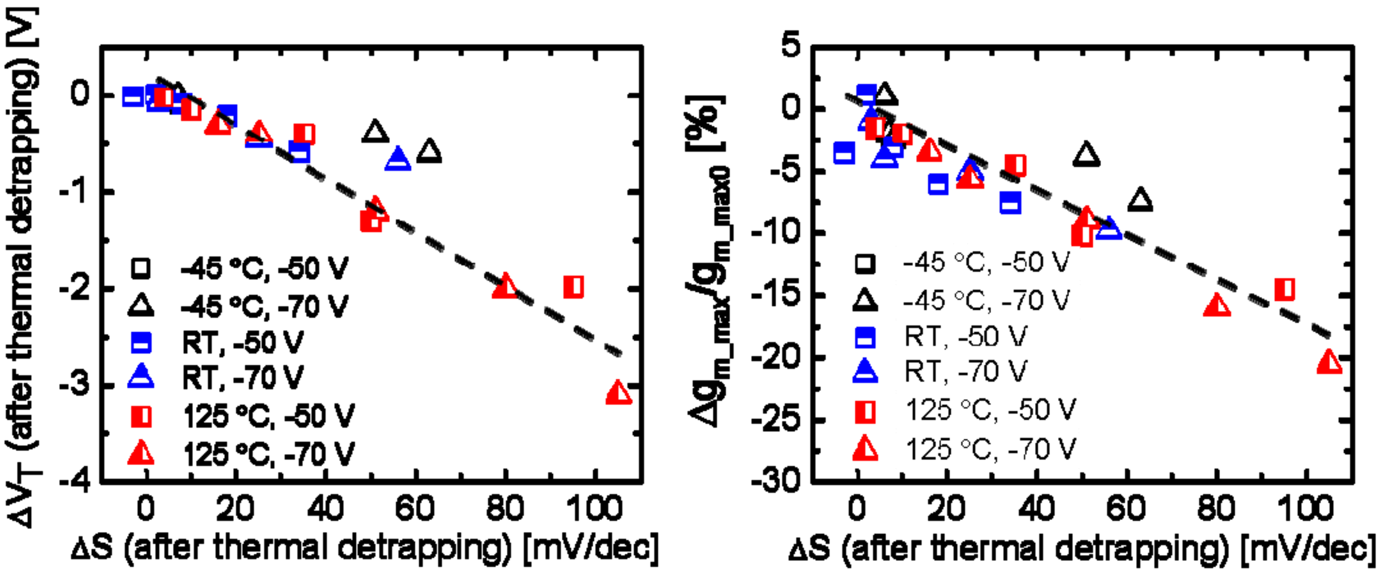
Stress conditions: $V_{GS.stress}$ = -10, -30, -50, -70 V; $V_{DS.stress}$=0; RT



$|V_{GS,stress}|$↑, t_{stress}↑ → permanent $|\Delta V_T|$↑, ΔS↑, $|\Delta g_{m,max}|$↑

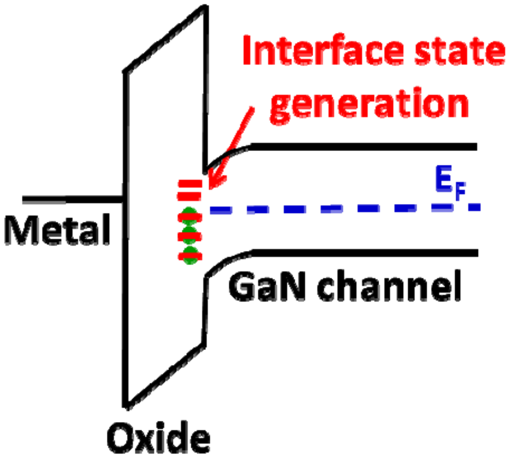
NBTI: Regime 3 (harsh stress)

Correlation of permanent ΔV_T, ΔS, $\Delta g_{m,max}$



- Consistent with interface state generation under harsh stress
- Observed in other MOS systems

  [i.e. Schroder, JAP 2007 in Si MOS]



Conclusions

- PBTI (benign stress):
  - ΔV_T , Δg_m due to electron trapping in pre-existing oxide traps
  - mostly recoverable
- PBTI (harsh stress):
  - additional permanent ΔV_T, Δg_m
  - generation of oxide traps near oxide/GaN interface

- NBTI (low stress):
  - recoverable $\Delta V_T<0$ due to electron detrapping from oxide traps
- NBTI (medium stress):
  - recoverable $\Delta V_T>0$, ΔS due to electron trapping in substrate
- NBTI (harsh stress):
  - non-recoverable $\Delta V_T<0$, Δg_m, ΔS
  - due to interface state formation